EUROPEAN PATENT OFFICE

Patent Abstracts of Japan

PUBLICATION NUMBER : 08064983
PUBLICATION DATE : 08-03-96

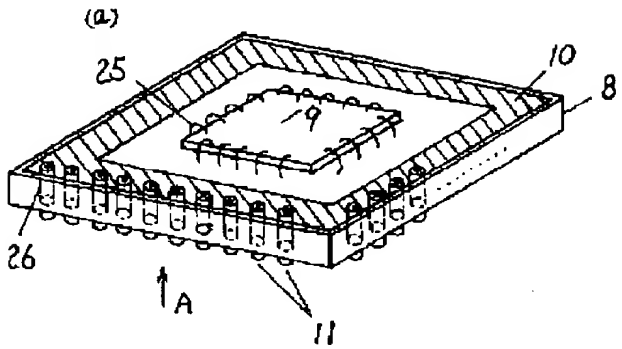
APPLICATION DATE : 25-08-94
APPLICATION NUMBER : 06200650

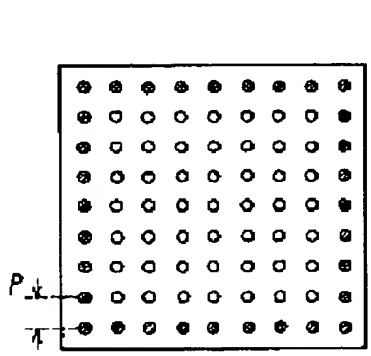
APPLICANT : MATSUSHITA ELECTRIC IND CO LTD;

INVENTOR : WATANABE TSUTOMU;

INT.CL. : H05K 9/00 H01L 23/12

TITLE : SHIELD CASE





ABSTRACT : PURPOSE: To prevent damages due to harmonic waves of a clock, data, etc., generated by an LSI using ground patterns of a BGA package and a main board.

CONSTITUTION: Grounds are made (at a connection terminal pitch) with through holes 26 in an outer part of an inner wiring board of a BGA constituted of two or more layers and a ground pattern 10 is formed in an outer part of a face of the BGA where a bare chip 9 is mounted. By covering the bare chip 9 with a shielding means, the BGA is shielded except signal power supply connection terminals 11. The shielded BGA is mounted on a main board 8 which is constituted of three or more layers. The entire surfaces of the front and rear face of the main board 8 are covered with ground patterns and many through holes 26 are made in an outer part of the main board to connect the ground patterns on the front and rear face. By this method, shielding can be conducted on the board 8.

PATENT ABSTRACTS OF JAPAN

(11)Publication number : **08-064983**

(43)Date of publication of application : **08.03.1996**

(51)Int.CI. H05K 9/00
H01L 23/12

(21)Application number : **06-200650**

(22)Date of filing : **25.08.1994**

(71)Applicant : **MATSUSHITA ELECTRIC IND CO LTD**

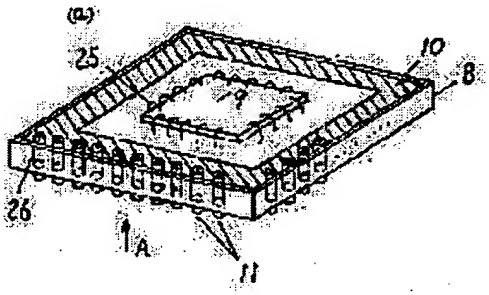
(72)Inventor : **YAMATE KAZUNORI**
WATANABE TSUTOMU

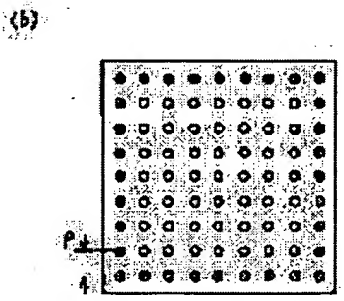
(54) SHIELD CASE

(57)Abstract:

PURPOSE: To prevent damages due to harmonic waves of a clock, data, etc., generated by an LSI using ground patterns of a BGA package and a main board.

CONSTITUTION: Grounds are made (at a connection terminal pitch) with through holes 26 in an outer part of an inner wiring board of a BGA constituted of two or more layers and a ground pattern 10 is formed in an outer part of a face of the BGA where a bare chip 9 is mounted. By covering the bare chip 9 with a shielding means, the BGA is shielded except signal power supply connection terminals 11. The shielded BGA is mounted on a main board 8 which is constituted of three or more layers. The entire surfaces of the front and rear face of the main board 8 are covered with ground patterns and many through holes 26 are made in an outer part of the main board to connect the ground patterns on the front and rear face. By this method, shielding can be conducted on the board 8.





LEGAL STATUS

[Date of request for examination]	14.06.1999
[Date of sending the examiner's decision of rejection]	
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	3082579
[Date of registration]	30.06.2000
[Number of appeal against examiner's decision of rejection]	

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]